Application No.: 09/764,487 Docket No.: 500.39521X00

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor memory device comprising two or more different types of memory cell arrays formed on a chip, at least two of the different types of said memory cell arrays being formed at different positions to each other in the vertical direction relative to said chip, wherein, when a memory cell array that takes a longer time to rewrite data, as one of said two vertically provided memory cell arrays, transfers its stored data to an external circuit, said stored data is transferred through the other memory cell array to the external circuit.

2. (Original) A semiconductor memory device according to claim 1, wherein at least a wiring conductor layer is interposed between said vertically formed memory cell arrays.

3. (Original) A semiconductor memory device according to claim 1, wherein data is transferred between said two vertically formed different memory arrays.

4. (Cancelled)

5. (Currently Amended) A semiconductor memory device ~~according to claim 1~~comprising two or more different types of memory cell arrays formed on a

chip, at least two of the different types of said memory cell arrays being formed at different positions to each other in the vertical direction relative to said chip, wherein the storage capacity of a memory cell array that takes a shorter time to rewrite data, as one of said two vertically provided memory cell arrays, is half that of the other memory cell array.

6. (Original) A semiconductor memory device according to claim 1, wherein one of said two vertically provided memory cell arrays has the function of a sense amplifier for the other memory cell array.

7. (Currently Amended) A semiconductor memory device ~~according to claim 1~~comprising two or more different types of memory cell arrays formed on a chip, at least two of the different types of said memory cell arrays being formed at different positions to each other in the vertical direction relative to said chip, wherein the upper one of said two vertically provided memory cell arrays does not need refresh operation, the lower one thereof needs refresh operation, and a logic circuit is provided at the same height as is the lower memory cell array.

8. – 17. (Cancelled)

18. (New) A semiconductor memory device according to claim 5, wherein at least a wiring conductor layer is interposed between said vertically formed memory cell arrays.

19. (New) A semiconductor memory device according to claim 5, wherein data is transferred between said two vertically formed different memory arrays.